



- Drafts
- Pending
- Active
 - L1: (2) ("20020054309").PN.
 - L2: (7514) network adj processor
 - L3: (111700) cache
 - L4: (743088) cam or (content adj address\$4 adj memory)
 - L5: (233) 2 and 3 and 4
 - L6: (22) 2 same 3 same 4
 - L7: (21980) shared adj memory
 - L9: (61) 8 not 6
 - L8: (63) 2 and 3 and 4 and 7
- Failed
- Saved
- Favorites
- Tagged (5)
- UDC
- Queue
- Trash

	U	1	Document ID	Issue Date	Pages	Inventor	Title	Current OR	Current XR
1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20030009651 A1	20030109	40	Najam, Zahid et al.	Apparatus and method for interconnecting a processor to a network using shared memory	712/34	
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20030147409 A1	20030807	13	Wolrich, Gilbert et al.	Processing data packets	370/412	
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20050268072 A1	20051201	35	Najam, Zahid et al.	Apparatus and method for interconnecting a processor to a network using shared memory	712/34	
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6311212 B1	20011030	10	Chong, Simon et al.	Systems and methods for on-chip storage of virtual connection descriptors	709/212	365/49; 370/282;
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 7082502 B2	20060725	31	Najam, Zahid et al.	Apparatus and method for interfacing with a high speed bi-directional network using a shared memory to store packet data	711/147	709/213; 709/253;

- Drafts
- Pending
- Active
 - L1: (689) (711/108).CCLS.
 - L2: (7514) network adj processor
 - L3: (743088) cam or (content adj address\$4 adj memory)
 - L4: (111700) cache
 - L5: (70) 2 and 1
 - L6: (17) 2 and 4 and 1
 - L7: (900) (711/148,153).CCLS.
 - L8: (17) 2 and 7
 - L9: (4537) (711/104,105,118,173).CCLS.
 - L10: (15) 2 and 3 and 4 and 9
 - L11: (2) 1 and 7
 - L12: (18) (2 and 3 and 4).clm.
- Failed
- Saved
- Favorites
- Tagged (5)
- UDC
- Queue
- Trash

U	I	Document ID	Issue Date	Pages	Inventor	Title	Current OR	Current XR
1	<input type="checkbox"/>	US 2003009651 A1	20030109	40	Najam, Zahid et al.	Apparatus and method for interconnecting a processor to processor using shared memory	712/34	
2	<input type="checkbox"/>	US 20030147409 A1	20030807	13	Wolrich, Gilbert et al.	Processing data packets	370/412	
3	<input type="checkbox"/>	US 20050268072 A1	20051201	35	Najam, Zahid et al.	Apparatus and method for interconnecting a processor to processor using shared memory	712/34	
4	<input type="checkbox"/>	US 63111212 B1	20011030	10	Chong; Simon et al.	Systems and methods for on-chip storage of virtual connection descriptors	709/212	365/49; 370/392;
5	<input type="checkbox"/>	US 7082502 B2	20060725	31	Najam; Zahid et al.	Apparatus and method for interfacing with a high speed bi-directional network using a shared memory to store packet data	711/147	709/213; 709/253